

CLAIMS

1. A semiconductor memory device comprising:
a storage element for storing information;
5 a constant current source for writing information into the storage
element by flowing current; and
a boost circuit for charging parasitic capacitors by a time when an
amount of a current flowed by said constant current source reaches an
amount of a current required to write information into the storage element,
10 at a predetermined position related to the storage element.
2. The semiconductor memory device according to claim 1, wherein
the storage element is a tunnel magnetoresistance element, and
the predetermined position may be a position where a magnetic field
by a current is applied to the tunnel magnetoresistance element.
- 15 3. The semiconductor memory device according to claim 1, wherein
said boost circuit comprises a condenser for storing charge to charge
the parasitic capacitors.
4. The semiconductor memory device according to claim 3, further
comprising a circuit for setting a voltage between both electrodes of the
20 condenser to a voltage greater than or equal to a power supply voltage.
5. The semiconductor memory device according to claim 3, wherein
a plurality of the condensers are provided, and
said boost circuit comprises switching means for switching a
condenser to be used for charging, according to an amount of charge
25 required to charge the parasitic capacitors.
6. The semiconductor memory device according to claim 5, wherein
the switching means switch a combination of condensers to be used for

charging, according to an amount of charge required to charge the parasitic capacitors.

7. The semiconductor memory device according to claim 5, wherein capacitances of at least a part of the condensers are mutually related by a
5 geometric progression.

8. The semiconductor memory device according to claim 5, wherein capacitances of at least a part of the condensers are determined according to capacitances of the parasitic capacitors depending upon an amount of a current required to write information into the storage element.

10 9. The semiconductor memory device according to claim 5, wherein capacitances of at least a part of the condensers are determined according to capacitances of the parasitic capacitors depending upon a position of the storage element.

10. The semiconductor memory device according to claim 5,
15 wherein capacitances of at least a part of the condensers are determined according to capacitances of the parasitic capacitors depending upon a process condition.

11. The semiconductor memory device according to claim 3,
comprising returning means for returning at least a part of charge on
20 parasitic capacitors which are present on a current path of a current for writing information into the storage element, to a node where charge of said boost circuit is stored.

12. The semiconductor memory device according to claim 3,
wherein a time when storing charge in said boost circuit is set at a time
25 after completion of an operation period of said constant current source.

13. The semiconductor memory device according to claim 1,
comprising charge retention means for retaining a part of charge on

parasitic capacitors which are present on a current path of a current for writing information into the storage element, in dependence on history of an operation mode, so as to suppress discharge of said boost circuit.